Characterization of High-Frequency GaN Circuits for Next Generation Wireless Systems

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Abstract: *This work presents an aggressive GaN-on-Si device model used to accurately predict transient switched-mode device behavior. The time-domain compatible, scalable, Angelov model is used to design a transformer-coupled class D switched-mode power amplifier. Simulation and measurement results report the GaN power device's intrinsic device efficiency to be 62% when operating as a switch at 2.25Gb/s. The 2-transistor PA topology demonstrates 29.5% efficiency at maximum power, and processes a single-carrier WCDMA waveform with -40.4dBc $ACPR_1$.*

Keywords: gallium nitride; RF; transmitters; power amplifiers; switched-mode; device model.

Introduction

With the evolution of CMOS, and advancements in novel digital signals processing (DSP) techniques, digital transmitters similar to that illustrated in Fig. 1 are beginning to show promise as an avenue for achieving the ubiquitous software radio, which processes numerous communications standards while maintaining high efficiency. Successful realization of these transmitters requires implementation of a high-efficiency 'digital' power amplifier (PA).

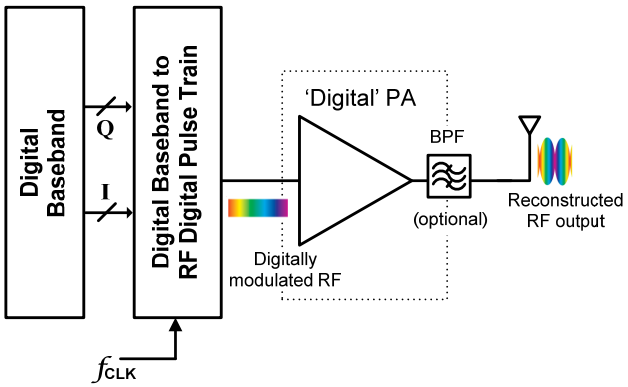

Figure 1. Digital RF transmitter.

Digital transmitters are not presently implemented in robust communication systems due to their inherent design challenges, including: efficient RF pulse modulation [1] and realization of a high-efficiency 'digital' PA capable of processing linear modulation schemes (e.g. WCDMA, OFDM). The main PA design challenges are: power device sizing to achieve both high output power and efficiency, and driver/interface design from the digital modulator to the PA. This work addresses these design challenges by implementing 1) a switched-mode PA in GaN-on-Silicon (GaN-on-Si) with integrated driver circuitry, and 2) an additional driver implemented on a commercial SiGe BiCMOS process.

Unfortunately, current GaN device models fail to predict (i.e. simulate) time-domain performance necessary for designing integrated switched-mode PAs and drivers with single-pass design success. Therefore, an aggressive modeling methodology is first presented and a device model is developed through RF characterization of the GaN-on-Si devices. The developed model is used to implement an RF switched-mode power amplifier.

GaN Device Model

Presently, GaN device models for simulating switched-mode (or digital) circuit performance suffer from the following limitations: 1) model is most accurate at DC bias points within the saturation region of the device, and operating the device in a switching operation invalidates the model, 2) model does not support time-domain (transient) simulations, since s-parameters are only fitted for 1 to 2 points, and 3) model does not scale with device size, therefore limiting min/max sizing and hampering designs for driver circuits [2],[3]. These limitations prohibit GaN models to be used for accurately predicting system-level circuit performance, particularly for switched-mode class D/E/F RF PAs.

This work employs a methodology for modeling GaN-on-Si devices by fitting a transient (time-domain) model to measured performance using a specified time-domain pulse mask. The DC model characteristics are fitted for I-V bias points falling within the region of switched-mode device operation, as illustrated in Fig. 2. The transient model correlation to measurements is verified using a rigorous TDT (time-domain transmissometry) measurement setup.

Device models were extracted from a series of GaN-on-Silicon HEMT test structures, ranging from 20μm to 4mm device size. Calibration structures were included on-chip to de-embed the test setup and on-chip pad parasitics. An extensive set of both static and pulsed IV and S-parameter measurements at multiple temperatures was performed to

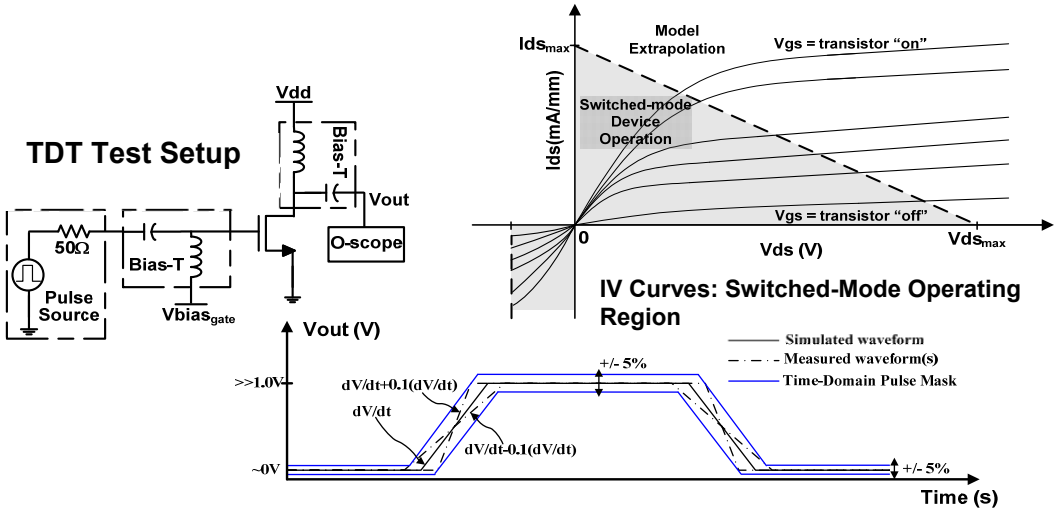

Figure 2. Measurement setup, I-V device operation for switched-mode applications, and time domain pulse mask requirements.

include self-heating effects within the device model. Furthermore, device model parameters were adjusted to meet the TDT mask. Measurements show good correlation to the scalable device model, down to 20µm device width. An example demonstrating the achieved correlation is shown in Fig. 5 for pulsed IV and S-parameters of a 1.2mm device. The S-parameter data spans a dynamic range from 200MHz to 25GHz.

In order to verify model accuracy for switched-mode PA applications, the measurement setup of Fig. 3 was used to characterize a single-stage differential mode GaN PA. An RF bit pattern of **2.25Gb/s** was applied directly to the gates of the GaN devices using an Agilent 13.5GB/s ParBERT with over 2V switching signal swing, and the instrinsic drain efficiency was measured by capturing the output signal through an Agilent ParBERT 13.5Gb/s N4873A Analyzer. The efficiency is calculated using *only* the output power for the fundamental tone (not broadband output power). Furthermore, the measurement setup includes the non-optimized load impedance provided by the discrete surface-mount output transformer, thus degrading efficiency. Fig. 4 reports the simulated and measured intrinsic drain efficiency for various signal powers *at node D* (does not include output network loss). The output power is baeked-off by decreasing the input signal's duty-cycle. The high accuracy between simulation and measurement results infers that the Angelov-based model predicts device switching behavior. This model has been used to design a switched-mode power amplifier, discussed in the following section.

Switched-mode Power Amplifier Design

Switched-mode PA Architecture: The most common switched-mode PA topologies are class D, E, and F, where class D RF configurations have been classified as both current and voltage mode [4],[5]. A simplified diagram of the class D architecture is shown in Fig. 6. The device(s)

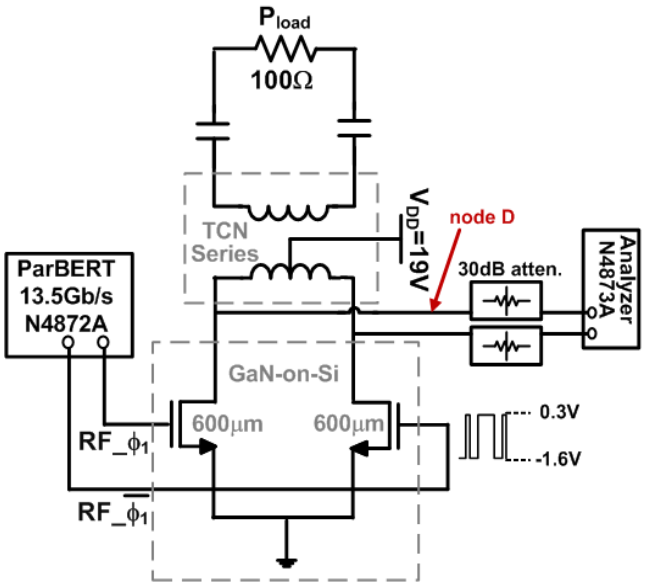

Figure 3. Measurement test setup for GaN switched-mode device power and efficiency characterization.

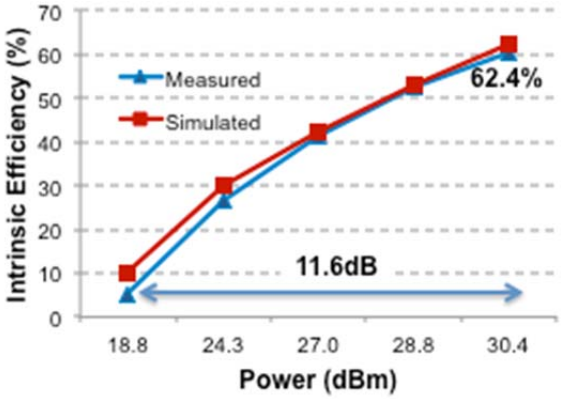

Figure 4. Measured Efficiency vs. Power for 600µm GaN differential switched-mode amplifier.

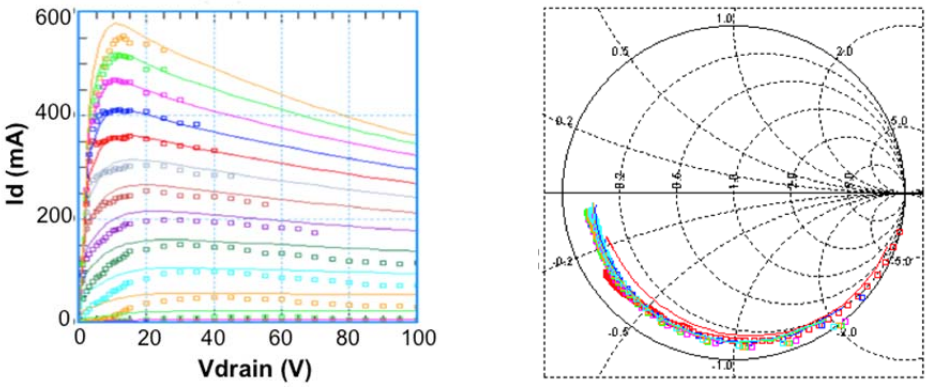

Figure 5. Pulsed IV and S-parameter measurement data. Sparameter: Vgs = -0.5 to 2.0, Vds=20V.

within a class D PA operate as switches and either the output voltage or current is shaped to a sinusoidal-like waveform, depending upon the output resonance network. An additional bandpass filter at the PA output is usually required to reconstruct the fundamental (desired) signal around the carrier frequency while removing harmonics caused by the switching operation. This architecture is limited to amplifying single-bit (1-bit) input signals, and oftentimes suffers from shoot-through loss and design complexity discussed in [4].

This paper presents a transformer-coupled voltage-mode (TCVM) class D power amplifier, with architecture illustrated in Fig. 7b, where the input signals, RF_ϕ_1 and RF_ϕ_2, are independently controlled. The advantages for choosing a transformer-coupled topology for implementation in GaN are: low-complexity driver circuitry, as the power devices do not have floating (source) nodes; reduction in shoot-through loss with asymmetric drive signals; and integration of a low-loss transformer network on GaN.

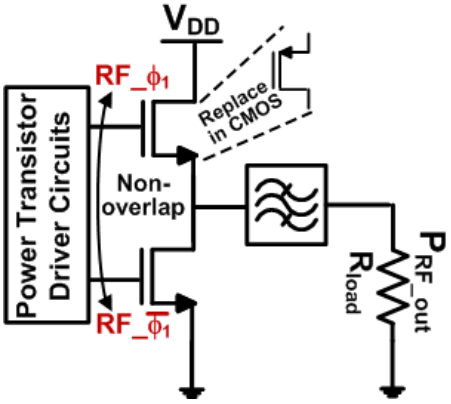

Figure 6. Class D PA architecture.

Furthermore, the 4-transistor topology allows for 1.5-bit signal amplification using the two RF inputs, as well as higher output power (for fixed V_{DD}) when compared with the 2-transistor topology shown in Fig. 7a. The potential improvement in transmitter efficiency, using 1.5-bit modulation shall be explained through an extended paper and GOMACTech 2014.

PA Driver Design: The power transistor driver circuitry was designed on Jazz 0.18µm SiGe BiCMOS. The driver consumes 1.6W and has the capability to directly drive 2mm GaN device widths. To the author's knowledge, this is the first reported driver that has been assembled with direct die-to-die connection without interface matching networks [6], as shown in Fig. 8.

Switched-mode PA + SiGe Driver Measurement Results: Since a custom integrated output transformer is required to efficiently realize the 4-transistor TCVM topology, preliminary measurements have been made using a 2-transistor topology similar to that of Fig. 7a. The measurement setup is comparable to Fig. 3, with the following differences: the GaN devices are 2mm width; the ParBERT is replaced by a SiGe driver integrated circuit (IC); and the power and efficiency measurements are taken at P_{load} (rather than node D), thus including output network loss. The output power (P_{load}) with 2.25Gb/s input signal is 32.6dBm. The system efficiency, including the driver and output network is 29.5%. With integration of the RF transformer and implementation of a 4-transistor topology, efficiencies above 50% are predicted in simulation results.

A single-carrier WCDMA signal was encoded into an RF digital pulse train using a 4:1 oversampling sigma-delta pulse modulator. The pulse train was used as an input signal to the SiGe BiCMOS driver. With 4:1 oversampling ratio, the desired RF output signal is centered at 337MHz. The measured and simulated PA output spectrum with the encoded WCDMA information is plotted in Fig. 9.

Conclusions

This work presents a GaN transient-based model used to predict switched-mode GaN device performance. The model demonstrates accurate prediction of device switching efficiency and power, and is used to design a

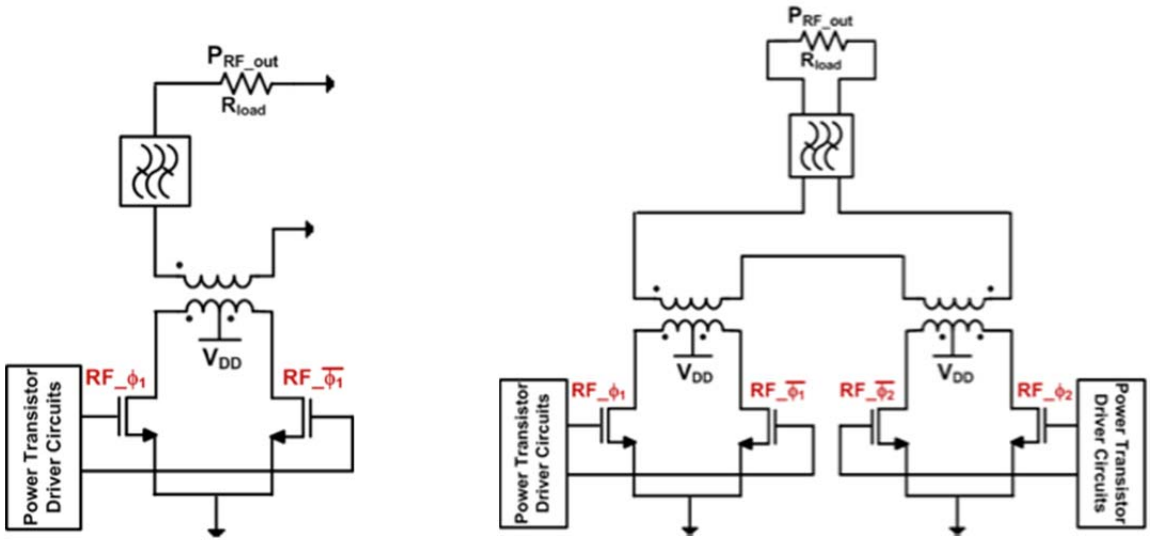

Figure 7. a) 2-transistor transformer-coupled voltage-mode (TCVM) class D PA, and **b)** 4-transistor TCVM class D PA.

transformer-couple class D power amplifier with driver circuitry implemented in SiGe. This work shall be extended to integrate the output transformer and move to larger GaN-on-Si power devices in an effort to achieve higher transmitter efficiencies.

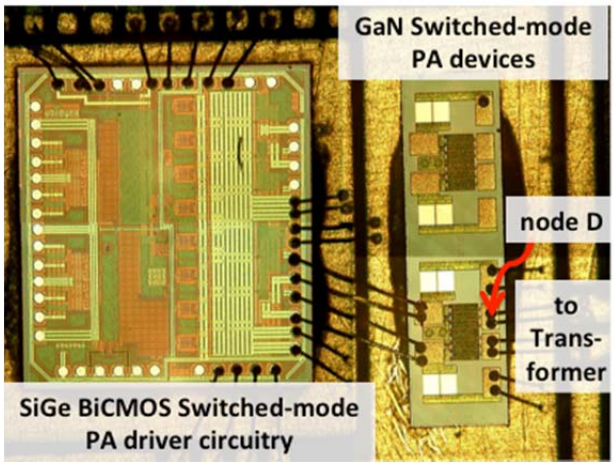

Figure 8. Switched-mode amplifier module.

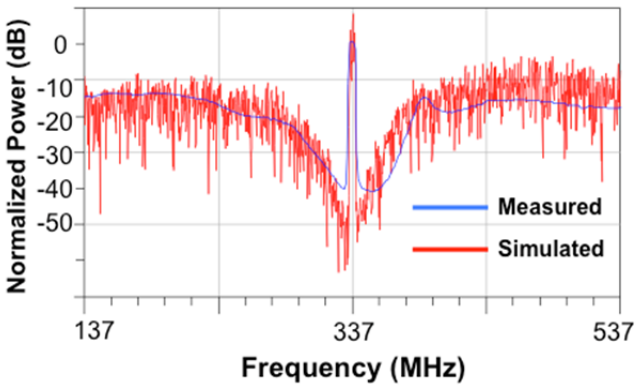

Figure 9. Measured and simulated PA Output Spectrum.

Acknowledgements

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